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Project SRAM – Design Review II

Report to PICo Review Board by
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SUBJECT: This document seeks to provide further evidence that our design meets the design requirements and specifications of the high-speed 64kb cache requested by the Portable Instruments Company (PICo).

Introduction

Portable Instruments Company (PICo) offered Very Large Scale Engineers (VLSE) a chance to win a substantial contract by demonstrating a specific type of SRAM—either 1 MB really low power (RLP) SRAM or a high-speed 64kb cache. We opted for the high speed cache, and this paper will prove that our designs show significant progress. Furthermore, this document shows that our design follows PICo's specifications for the high-speed cache. Our design choices are shown below, with substantial evidence that our design choices are justified. We look forward to feedback from PICo, so we can continue with our key optimizations and meet the December 3 deadline.

In this paper, we also provide our weekly timeline and milestone breakdown from the project proposal, with annotations regarding progress, and our newly updated milestone breakdown. With this, we also provide our remaining challenges moving forward. We also provide the status of each block component in our proposed SRAM design. Furthermore, we provide simulations for our proposed design, specifically using a scaled version of the SRAM (specifically a 2x2 block) since it is infeasible to efficiently simulate for an entire 64kb cache. The overall results show promise and can be extrapolated to mean if we wire the entire 64 kb SRAM design together, the results should be similar. Although the larger schematics have not yet been created, we have created smaller representative schematics and smaller layouts, once again revolving around the fact that they simply need to be wired together for the larger block versions. Lastly, our references can be found at the end, and schematics, simulations, and layout images can be found in our Appendix.

Design

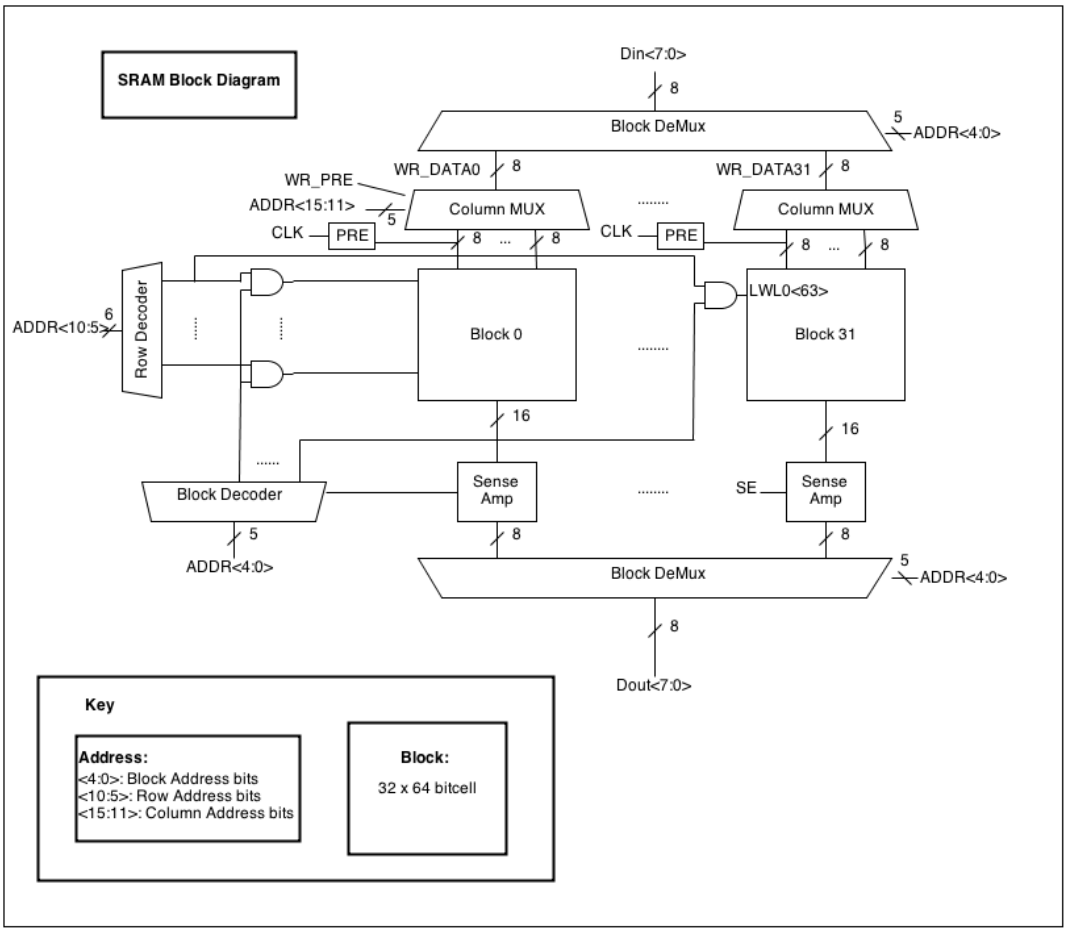

Figure 1: Block Diagram that our design follows

Table 1: Completion Status of each block of Block Diagram

Component	**Schematic**	**Layout**	**Simulation**
SRAM 6T Bitcell	Completed	Completed	Completed
Sense Amp	Completed	Incomplete	Completed
AND Gates	Completed	Completed	Completed
SRAM Blocks	Completed	Completed	Completed
1-to-32 Block DeMUX	Completed*	Completed*	Completed*
32-to-1 Column MUX	Completed*	Completed*	Completed*
Row Decoder	Completed**	Completed**	Completed**
Block Decoder	Completed**	Completed**	Completed**

Overall, we have completed the majority of the schematics and testing simulations. We have completed schematics and simulations for the SRAM bitcell, the sense amp, the AND gates, and the SRAM blocks (32x64 bit cells). As the layout of the full blocks of SRAM is simply a tiling, our layout for 1 bit cell should be sufficient as a layout for the bit cell array. As an example, we have attached a layout of a 2x2 array of bit cells.

*We do not have the full schematics for the DeMUX and MUX. However, we have schematics and working simulations for the 1 bit variants (1-to-2 DeMUX and a 2-to-1 MUX). We have the schematics for the full versions designed; they simply need to be implemented. As far as layouts go, these components are designed using transmission gates. We have a layout for transmission gates so a simple tiling and routing (connecting) should suffice for each of the components' respective layouts. We chose to use transmission gate DeMUX and MUX architectures because of the metric payoff. The transmission gates save a lot of area, reduce leakage, and improve speed when compared to the static cmos counterparts.

**Similar to the MUX and DeMUX situation. We have the row and block decoders designed and simulated for the 2x2 bit cell array. As such, these need to be expanded to be able to handle the full bit cell array. Again, these decoders were designed using only transmission gates, so we believe the layout to be solely a tiling and routing.

Design Simulation

In order to simulation our proposed design, we decided it would be worthwhile to create and test a 2x2 bit cell array. We believe that this is an effective representation of the whole project as it utilizes all the same concepts and components, simply to a smaller scale. We believe that the functionality of the final project should mirror the functionality of our test array. The setup used for simulation can be found in figure 2 below. More in depth schematics of each of the components found in figure 2 can be found in the appendix (in figures 4, 5, and 6).

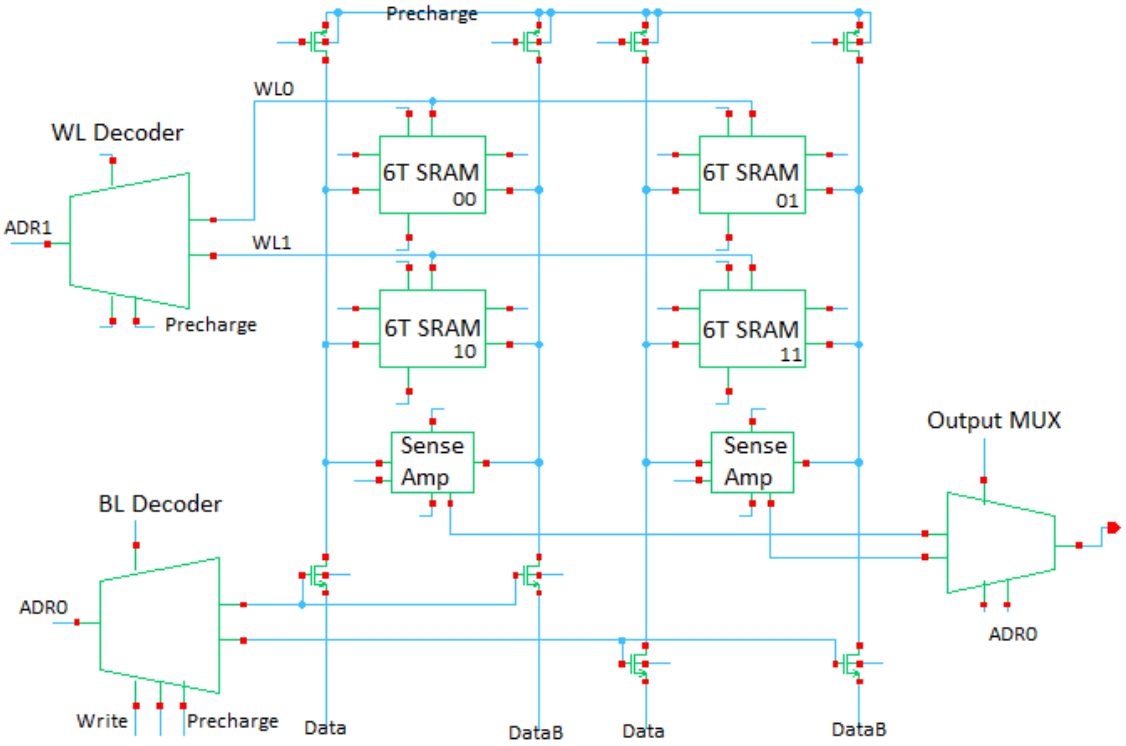

Figure 2: 2x2 Block Schematic for Simulation

We decided that the most useful simulation to show functionality was to write 3 times to the 01 bit cell, and then write 3 times to the 10 bit cell. This would test each wordline and set of bitlines at least once and show that both the BL and WL decoders were functioning. Upon testing, we were ultimately pleased with the results. The writes appeared to have worked correctly without errors. The only issue was glitches in the plots but nothing significant. The simulations results are shown in the appendix figures 7, 8, and 9. This was the nominal simulation. We then decided it would be useful to test our model at the process corners. The results of those tests are summed up in Table 2 below. The plots can be found in the appendix (the input plot is the same as the previous nominal simulation (Figure 7).

Table 2: Process Corner Simulation Results

PMOS	**NMOS**	**Results**
Slow	Slow	Worked with minor glitches in plot. (Figures 10 and 11)
Slow	Fast	Worked with minor glitches in plot. (Figures 12 and 13)
Fast	Slow	Mostly worked. However, 1 of the 6 writes failed. The value of the 01 bit cell failed to write the 1 for the last of its 3 transitions. On the plot, see it starting to pull up, but ultimately fails. (Figures 14 and 15)
Fast	Fast	Worked with minor glitches in plot. (Figures 16 and 17)

The failures in the Fast-Slow process corner leads us to believe that we still have issues in our bit cell sizing ratios. We will have to revisit the sizing again in the future. Also, we noticed a lot of spiking and glitching at the final read output at the very start of the rise of a read cycle. It is suspected to be caused by overlapping input signals with non-ideal rise/fall times.

Layout

Compared to our previous layouts we have been able to make significant improvements in the areas of cell-to-cell interface, symmetry, and compactness. We believe our new layout conforms to industry standard with VDD and VSS supply rails that can be shared across bit cells and enable area efficient tilling. The taps have been moved to bit cell edges, so when tiled they are easier to connect together. For now in the 6TSRAM (Figure 18) and 2x2 6TSRAM (Figure 19) Layouts do not show the taps being shared across cells as we do not feel it is necessary to add extra clutter at this stage of design. In the layout of the single SRAM cell we found it better to share one NTAP and one PTAP for the sets of NMOS's and PMOS's. We found this to be a better approach because adding the NTAP wire does saves us from need to input another tap and keep the nets connected. Having two NTAP or PTAP nets decided would be unnecessary and thus scrapped the design.

The transmission gate (Figure 20) and inverter (Figure 21) layouts are complete. As most of our parts contain transmission gates and inverters, most of the layout is completed, with the only major requirement being the creation of the Sense Amplifier in layout. This has not been checked off yet because it does not require just a simple connection of transmission gates and inverters.

Remaining Challenges

The primary remaining challenges involve smoothing out glitching and finishing the layout for the Sense Amp and MUX/DeMUX. The layout for the Sense Amp is currently in process, but issues with Cadence have prevented us from completing the Sense Amp layout (specifically, issues when running the LVS). The layout for the Sense Amp design is not complex by any means, so this is not a huge priority at the moment. Our schematics for the Sense Amp simulate well, so we will optimize the Sense Amp for the final design and provide the layout then.

These issues with LVS also appear elsewhere in our layout creation, and therefore we will need to ensure we can mitigate these issues. We will meet with members of PICo's technical staff to figure out the cause and solution of these issues.

One of our process corners does not work (as seen in Table 2), which is an issue that is our first priority. We are currently calculating the necessary sizes that may fix this.

Another challenge we are running into involves signal-to-noise margin (SNM) simulations and Monte Carlo simulations. Specifically, we have attempted to conduct these simulations, but our results have shown there is an error in our method. Therefore, we need to further refine our method for these simulations, as these are important metrics to calculate because they measure the probability of error.

Lastly, our remaining challenge is to complete optimizations on the working circuit. We seek to optimize as much as possible, so our 64kb high speed cache design is on the Pareto frontier with respect to power, size, and delay.

Proposal Project Timeline and Milestones (Weekly)

Our milestone list was based on an initial misunderstanding of requirements for Design Review II. At first, we thought the optimizations were due for Design Review II, but we discovered that was not the case, so we are still in the process of optimizing our components and reviewing current optimizations.

Note: bolded milestones on schedule are customer deadlines (i.e. Design Reviews, Presentations)
Note: strikethroughs indicate completion

- Oct 13 - 19
  - ~~Oct 16: Optimize layout before beginning speed optimizations~~
  - ~~Oct 16: Ensure all simulations show functional SRAM cell~~
  - ~~Oct 16: Finish proposal for PICo~~
  - ~~**Oct 17: Submit proposal to PICo**~~
- Oct 20 - 26
  - ~~Oct 20: Begin in depth learning of SKILL and writing Ocean scripts~~
  - ~~Oct 21: Connect all components together and simulate~~
  - ~~Oct 22: Calculate initial pre-optimization metrics~~
  - ~~Oct 24: Begin designing schematics for high speed optimizations~~
- Oct 27 - Nov 2
  - Oct 28: Conduct simulations on optimized schematics
  - Oct 29: Begin connecting components together and testing
- Nov 3 - 9
  - Nov 3: Ensure all components are connected and tests show optimized functionality
  - Nov 4: Finish layout for optimized SRAM
  - Nov 9: Finish process corner simulations for optimized SRAM
- Nov 10 - 16
  - Nov 11: Ensure all simulations show optimized functionality for SRAM
  - Nov 11: Finish report for Design Review 2
  - **Nov 12: Submit Design Review 2**

- Nov 17 - 23
    - Nov 17: Finish Design and basic simulations
    - Nov 21: Finish process corner simulations
    - Nov 22: Calculate design metrics and process corner metrics
    - Nov 23: Finish layout for entire design
- Nov 24 - 30
    - Nov 26: Ensure all simulations are accurate and represent our design well
    - Nov 28: Write final design report and presentation for PICo
- Dec 1 - 5
    - **Dec 3: Ensure everything is finalized and prepared for delivery**
    - **Dec 3 or 5: Present Design to PICo**

Updated Project Timeline and Milestones (Weekly)

Note: bolded milestones on schedule are customer deadlines (i.e. Design Reviews, Presentations)

- Nov 10 - 16
    - Nov 11: Ensure all simulations show optimized functionality for SRAM
    - Nov 11: Finish report for Design Review 2
    - **Nov 12: Submit Design Review 2**
    - Nov 15: Finish design of optimized schematics and begin basic simulations
- Nov 17 - 23
    - Nov 16: Finish learning SKILL and use SKILL and ocean scripts as much as possible
    - Nov 18: Conduct Monte Carlo analysis and SNM analysis on individual components
    - Nov 21: Finish process corner simulations
    - Nov 22: Calculate design metrics and process corner metrics
    - Nov 23: Finish layout for entire design
- Nov 24 - 30
    - Nov 24: Connect all components together and simulate
    - Nov 18: Complete Monte Carlo analysis and SNM analysis on entire connected SRAM
    - Nov 25: Complete process corner simulations
    - Nov 26: Ensure all simulations are accurate and represent our design well
    - Nov 28: Write final design report and presentation for PICo
- Dec 1 - 5
    - **Dec 3: Ensure everything is finalized and prepared for delivery**
    - **Dec 3 or 5: Present Design to PICo**

References

1. Rabaey, J., Chandrakasan A., Nikolic, B., *Digital Integrated Circuits (2nd Edition)*, (Dec 24, 2002)
2. Calhoun, B., *Design Principles for Digital CMOS Integrated Circuits*, (March 7, 2012)
3. Cash L., Duan C., Reed R., Tyler A., *Design Review 1, Los tOHMales Callentes, VLSI 4332*, (Oct 5, 2012)
4. Bailey S., Linger K., Lorenzo R., Thompson J., *Project SRAM - Design Review 1*, (Oct 2012)
5. *Design And Analysis Of Sense Amplifier*, http://www.projecttopics.info/Computer/Design_And_Analysis_Of_Sense_Amplifier.php
6. Jacob, B., Ng, S. W., & Wang, D. T. *Memory systems: cache, DRAM, disk,* Burlington: Morgan Kaufmann, 2007, 282.
7. Amrutur, B., *Design and Analysis of Fast Low Power SRAMs*, (Aug 1999)
8. Prabhu, C.M.R., *Low-power fast static random access memory cell*, (Dec 2010)
9. US 7499312: "Fast, stable, SRAM cell using seven devices and hierarchical bit/sense line"
10. US 5604712: "Fast Word Line Decoder for Memory Devices"
11. US 5991217: "Fast SRAM Design Using Embedded Sense Amps"
12. US 7143257: "Method and Apparatus of a Smart Decoding Scheme for Fast Synchronous Read in a Memory System"

Appendix

Printouts

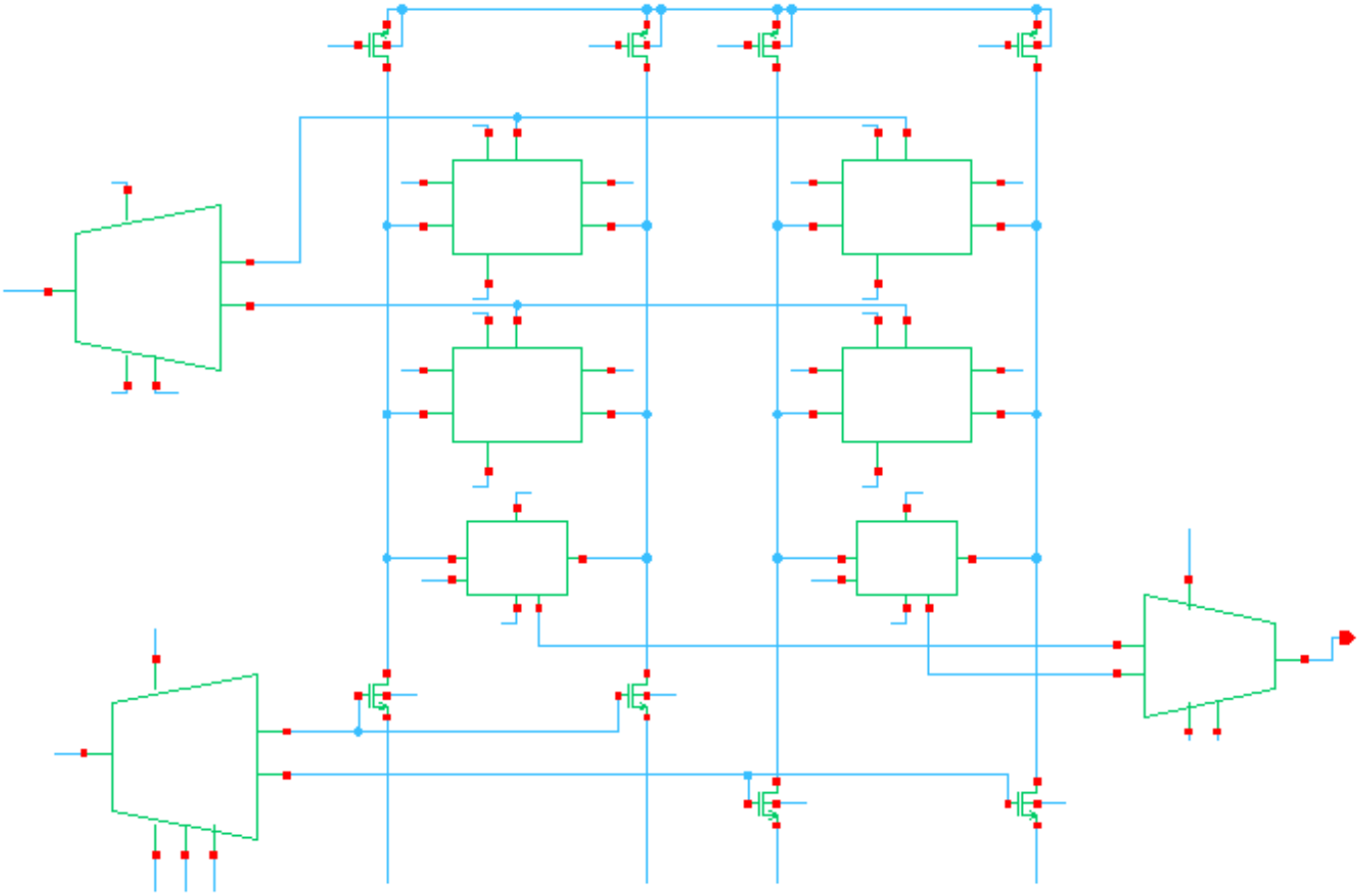

Figure 3: 2x2 Block Diagram Schematic

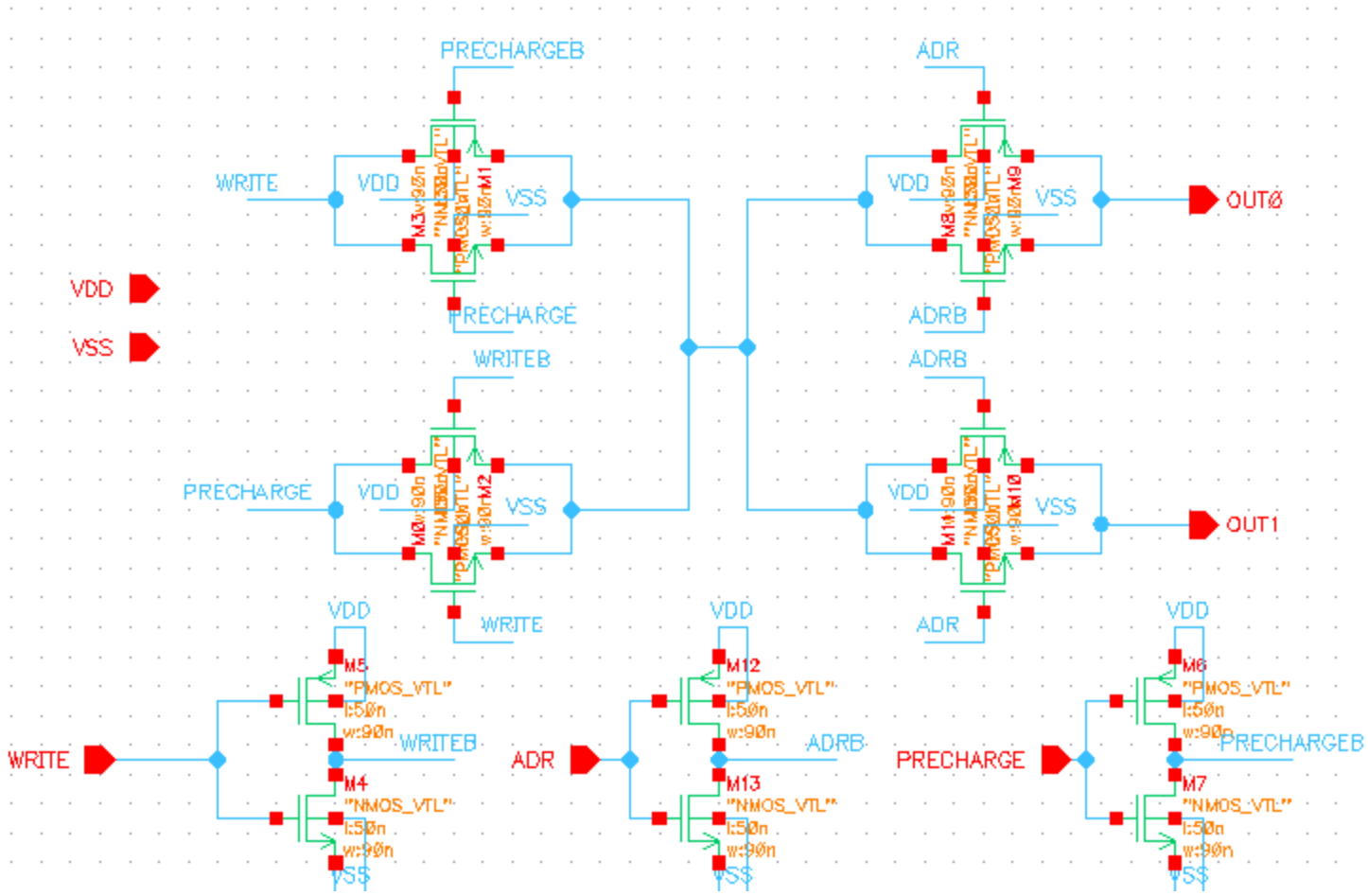

Figure 4: Bit-Line Decoder

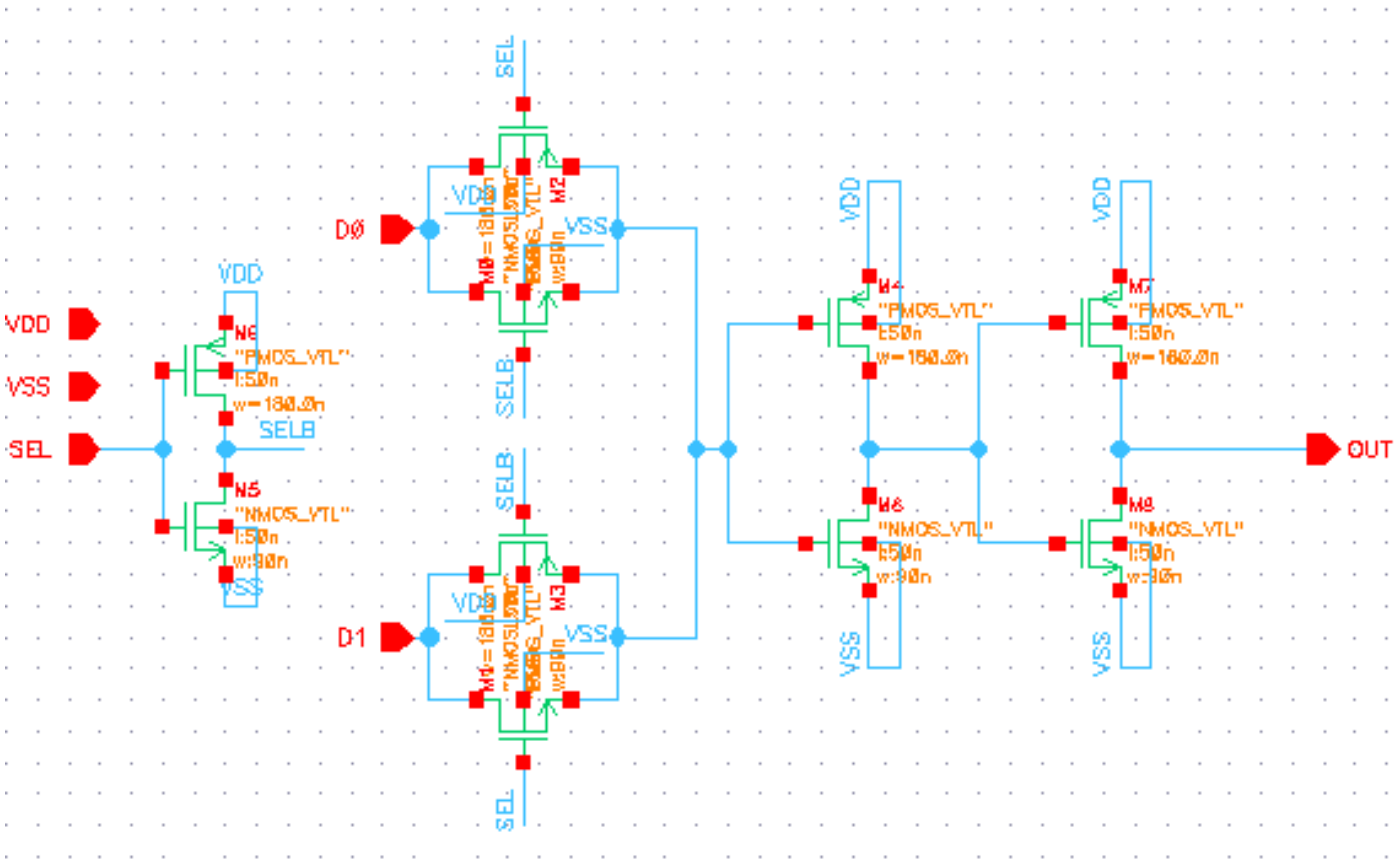

Figure 5: Output MUX

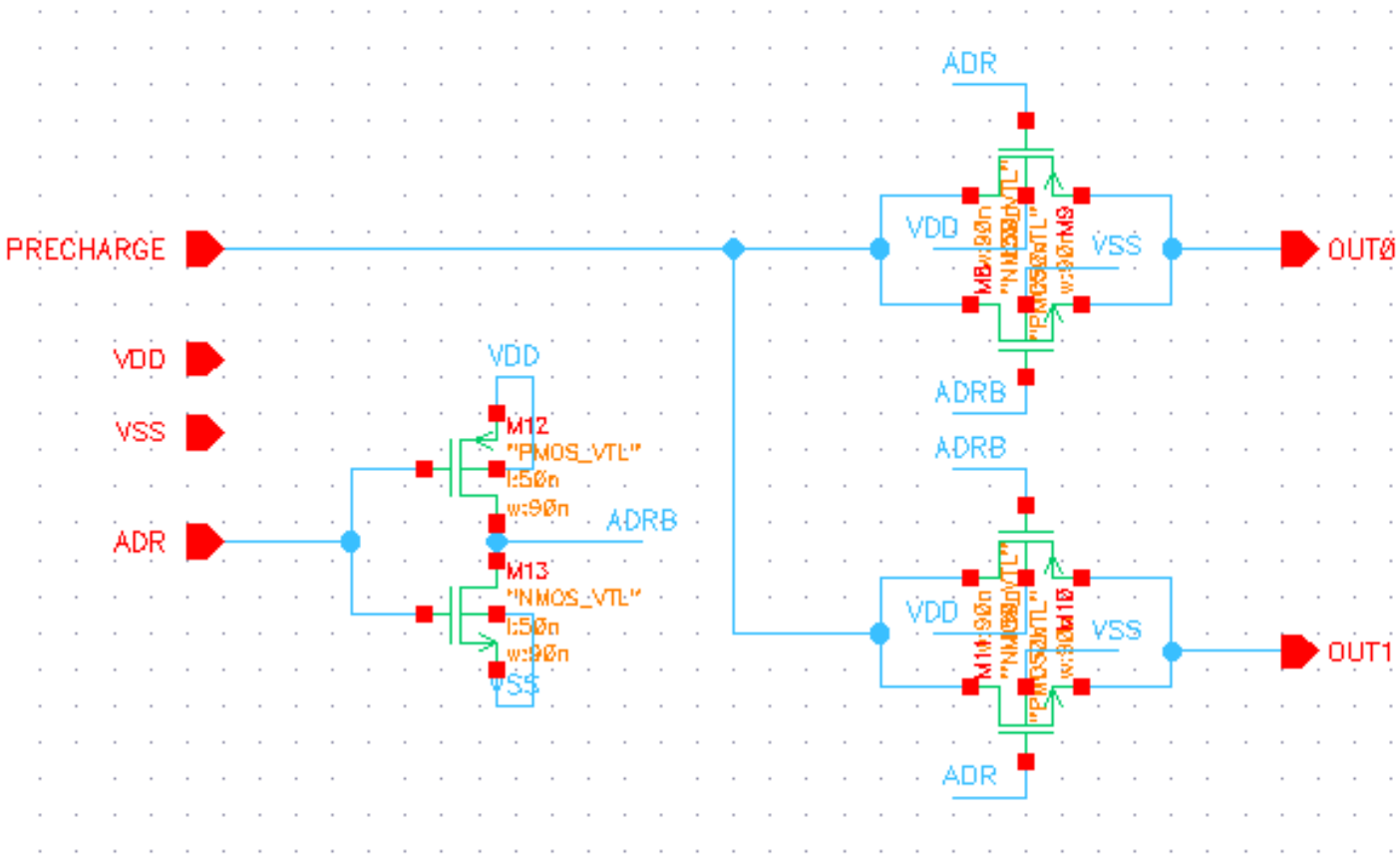

Figure 6: Word-Line Decoder

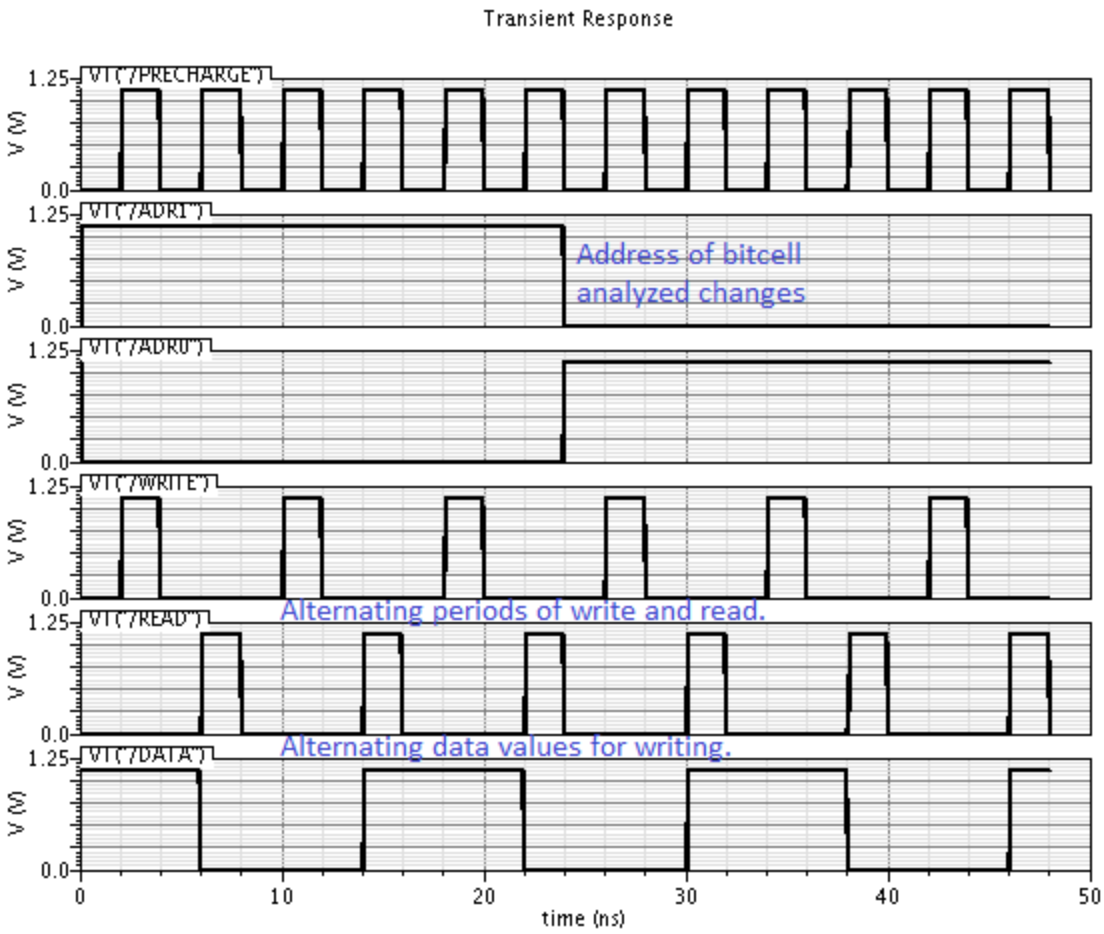

Figure 7: Simulation Inputs

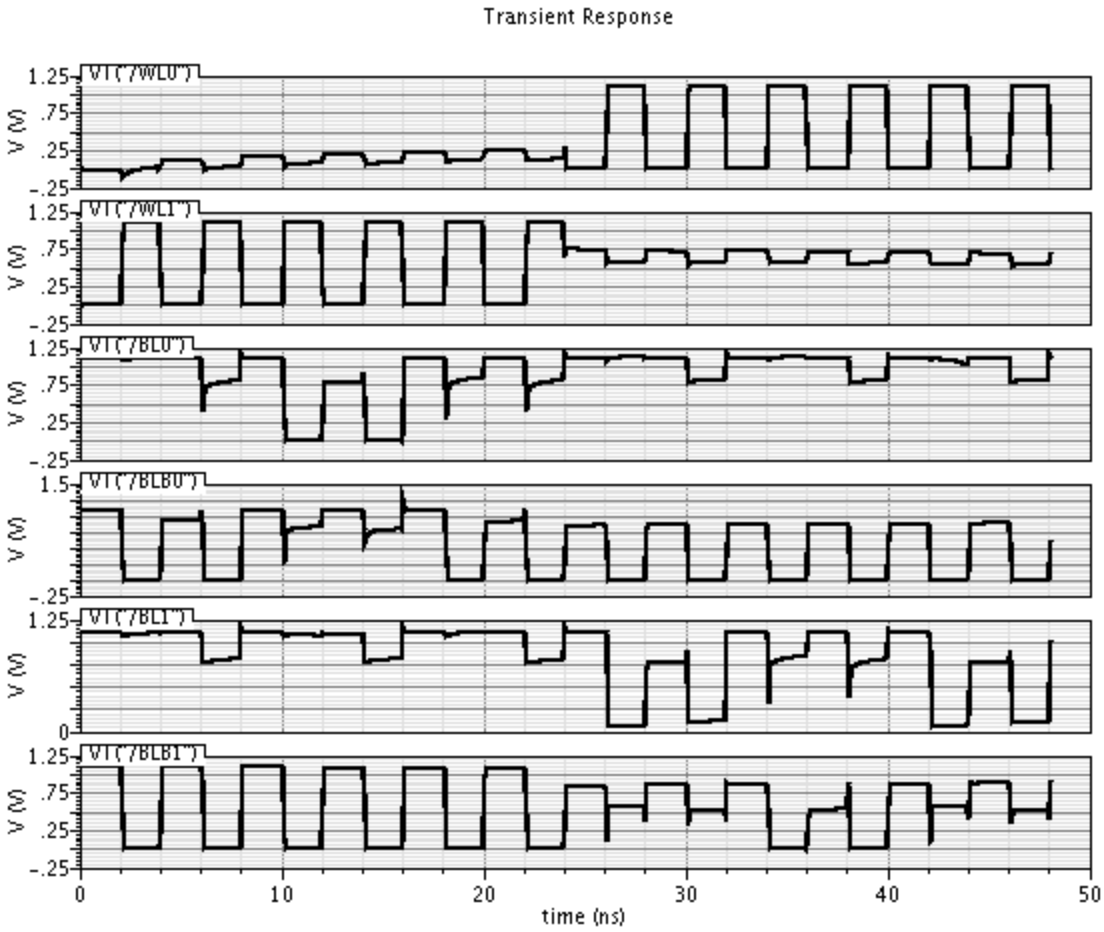

Figure 8: Simulation Intermediates

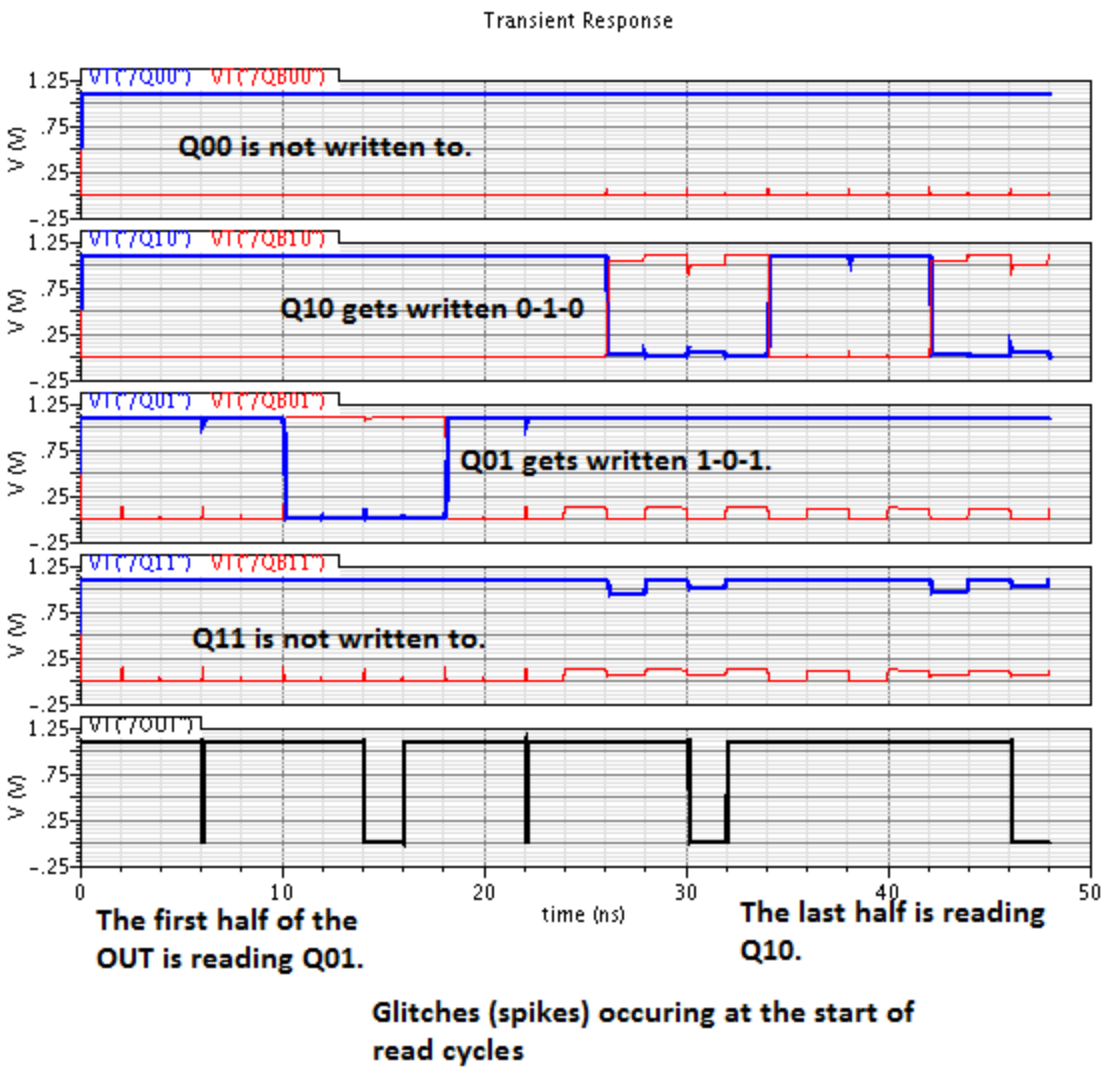

Figure 9: Simulation Outputs

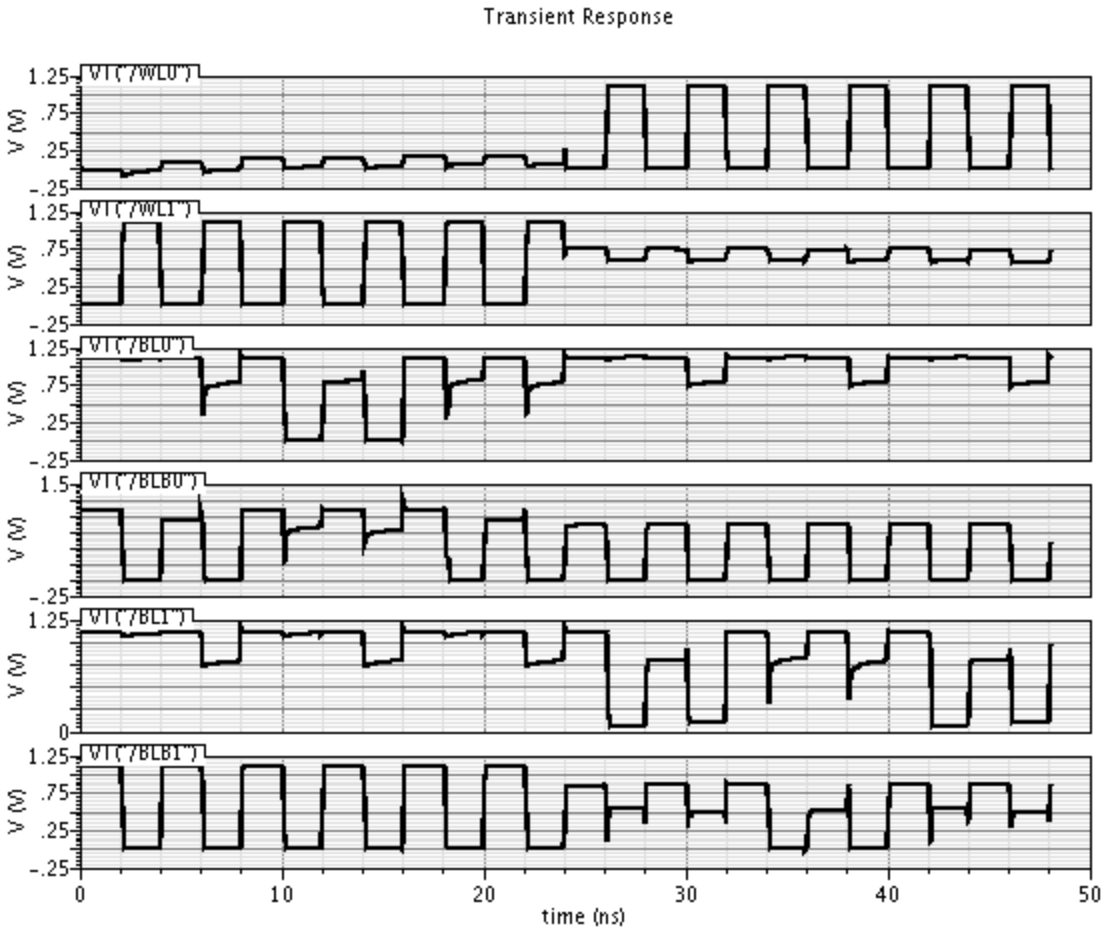

Figure 10: Intermediates of Slow-Slow Process Corner

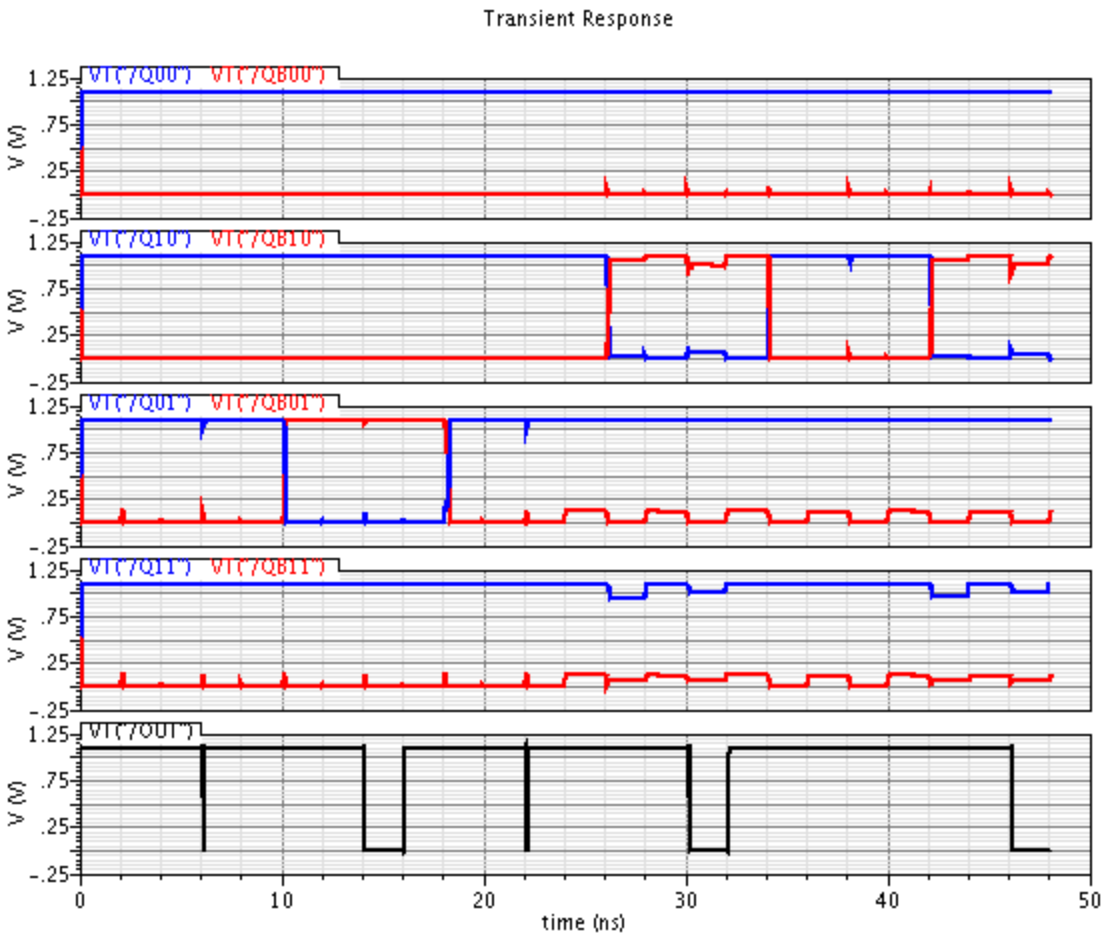

Figure 11: Outputs of Slow-Slow Process Corner

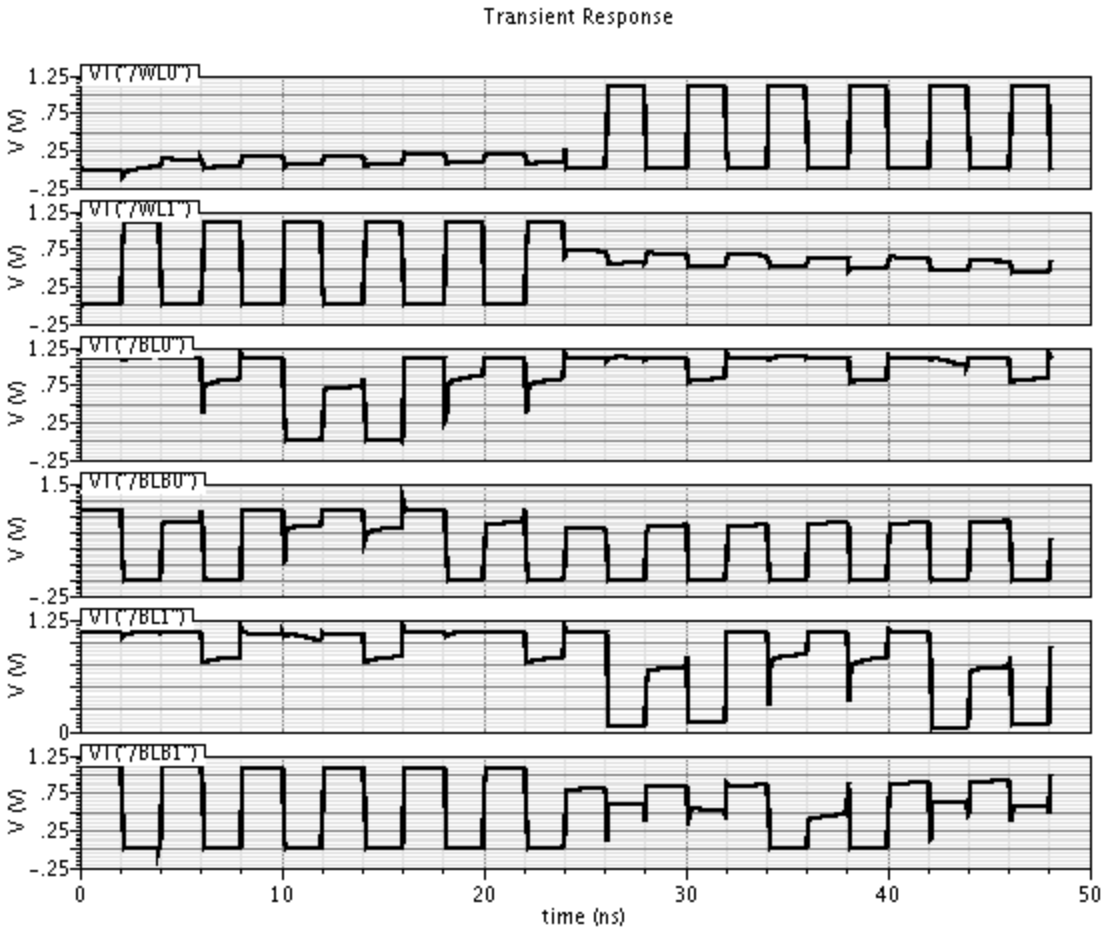

Figure 12: Intermediates of Slow-Fast Process Corner

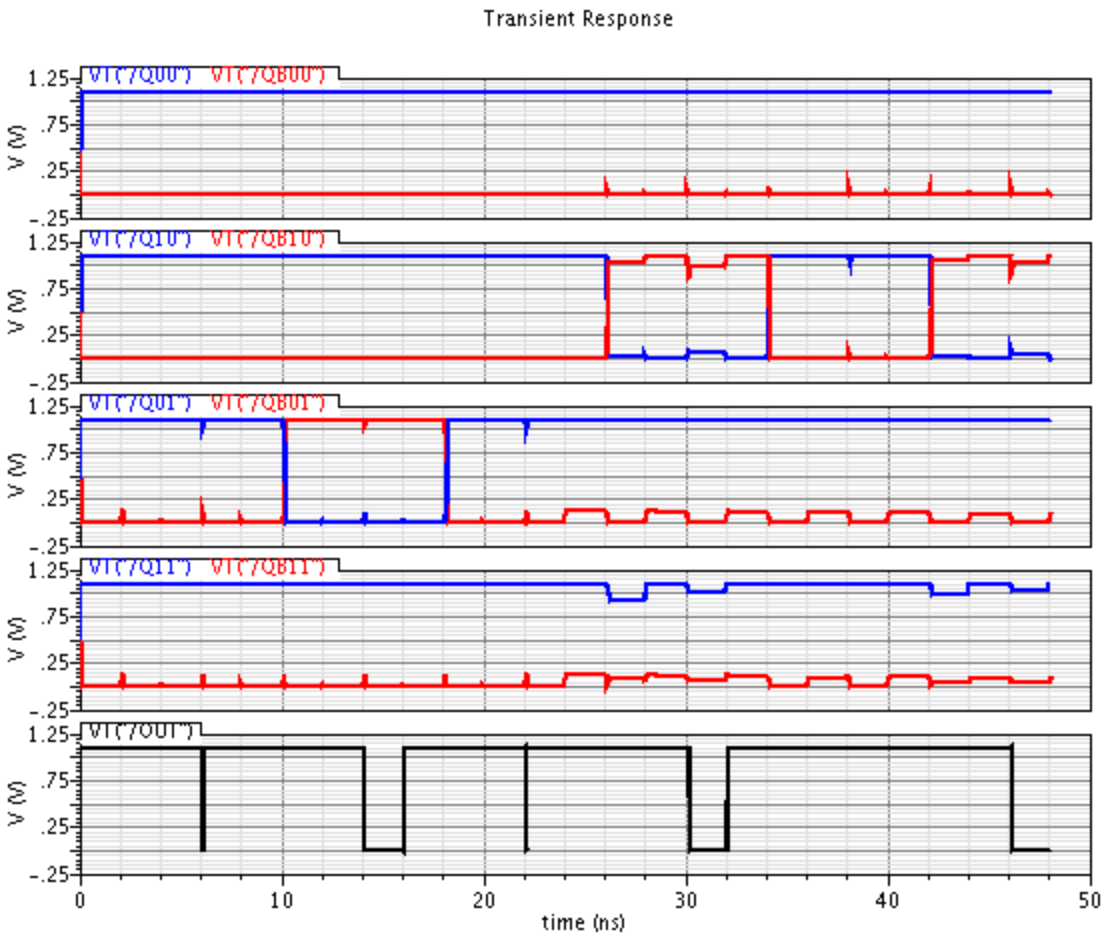

Figure 13: Outputs of Slow-Fast Process Corner

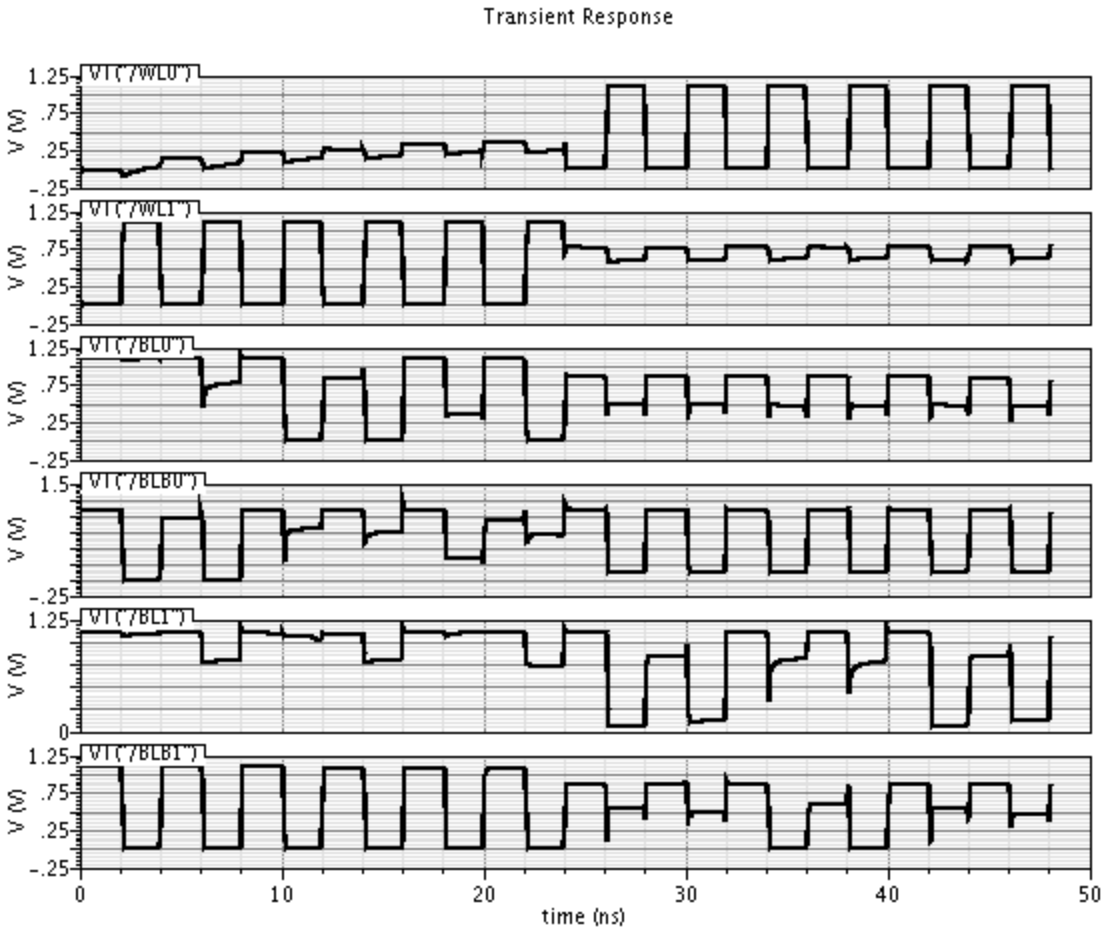

Figure 14: Intermediates of Fast-Slow Process Corner

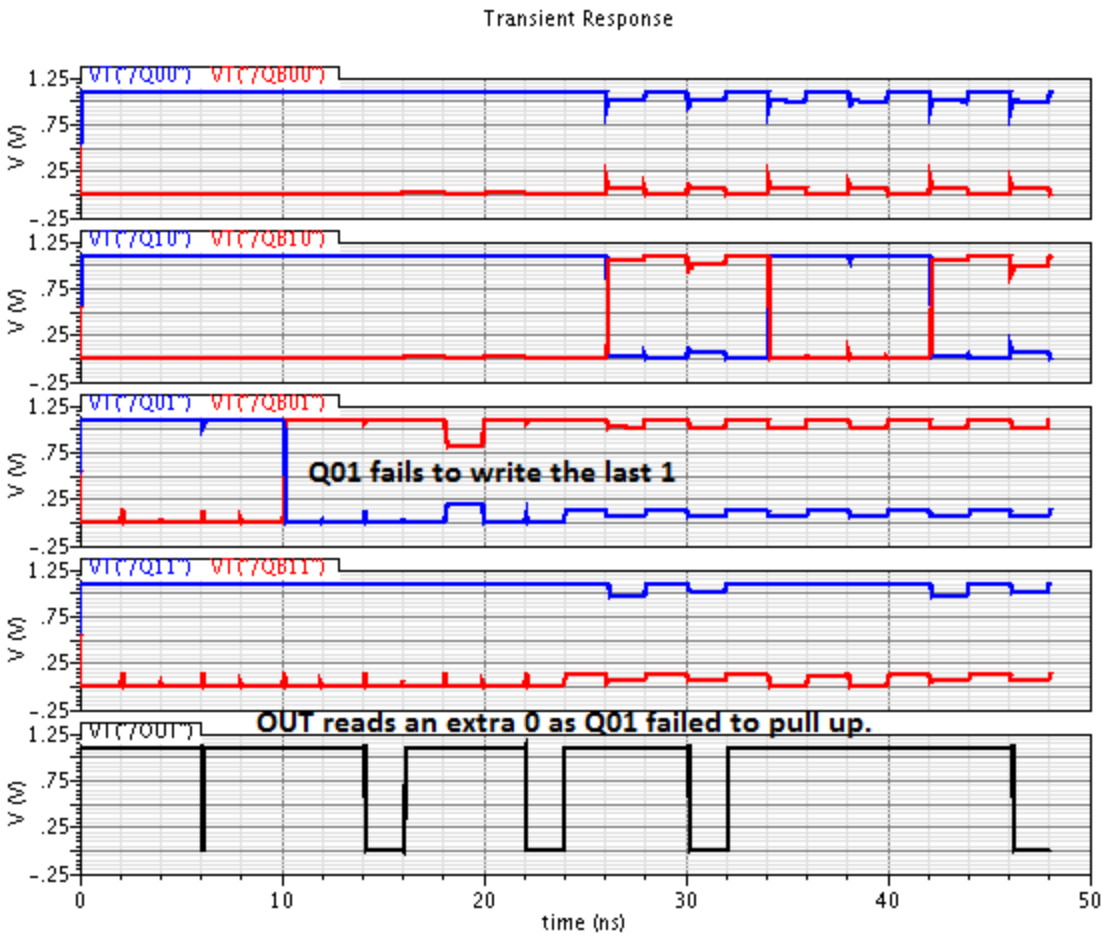

Figure 15: Outputs of Fast-Slow Process Corner

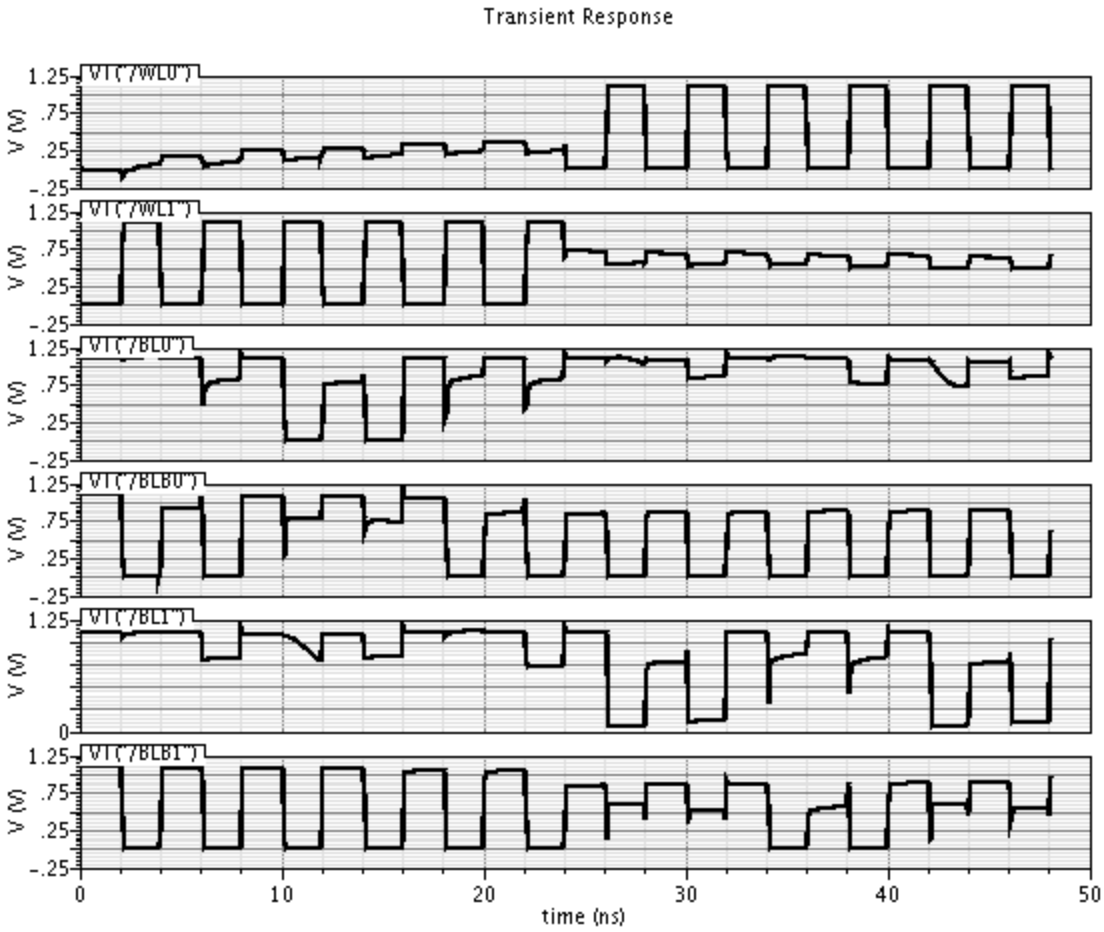

Figure 16: Intermediates of Fast-Fast Process Corner

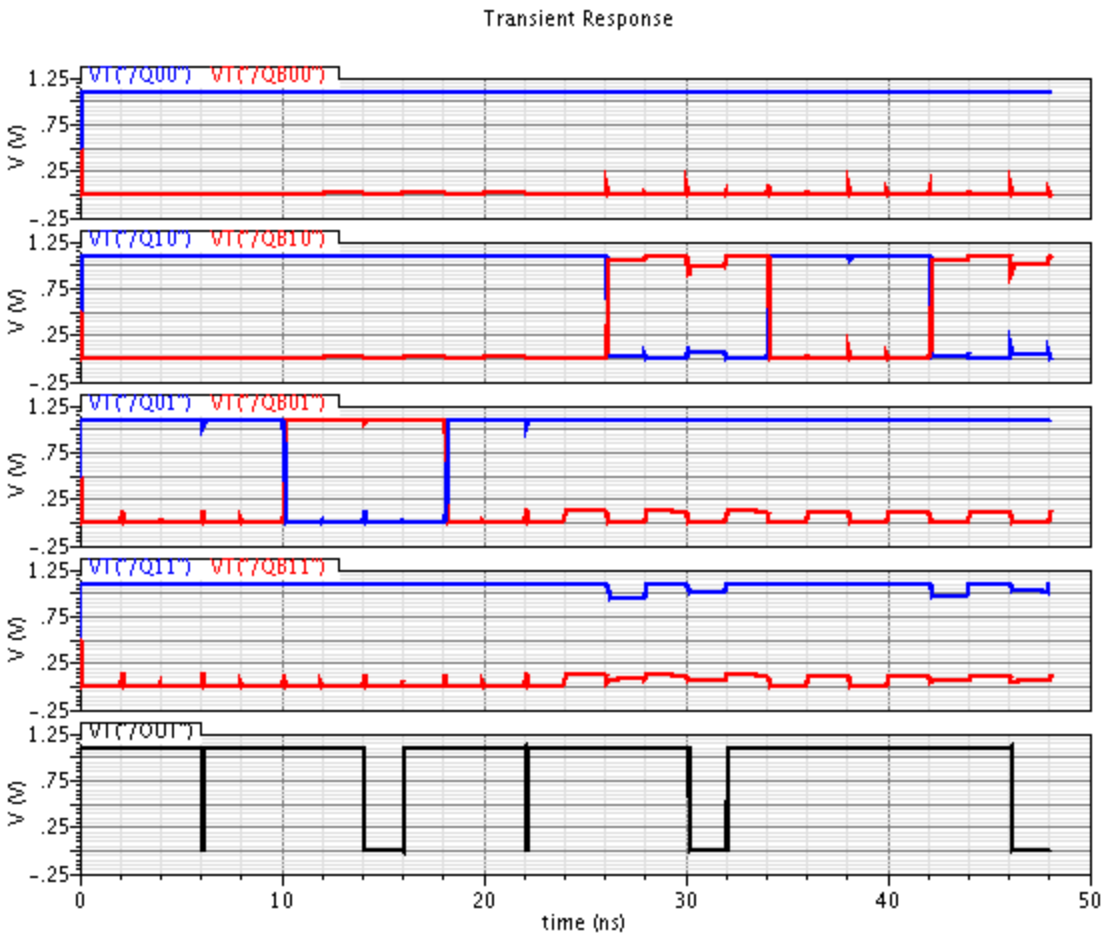

Figure 17: Outputs of Fast-Fast Process Corner

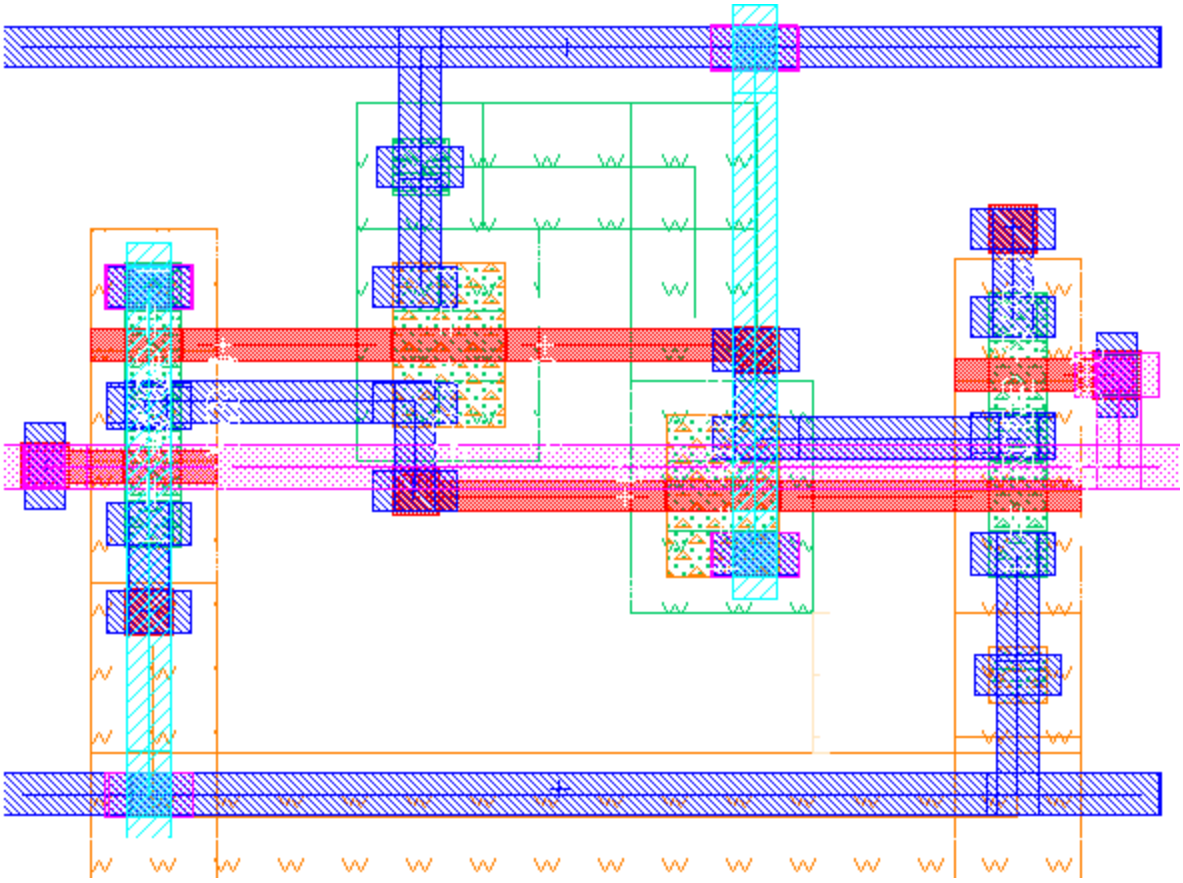

Figure 18: Layout of 6T SRAM Cell

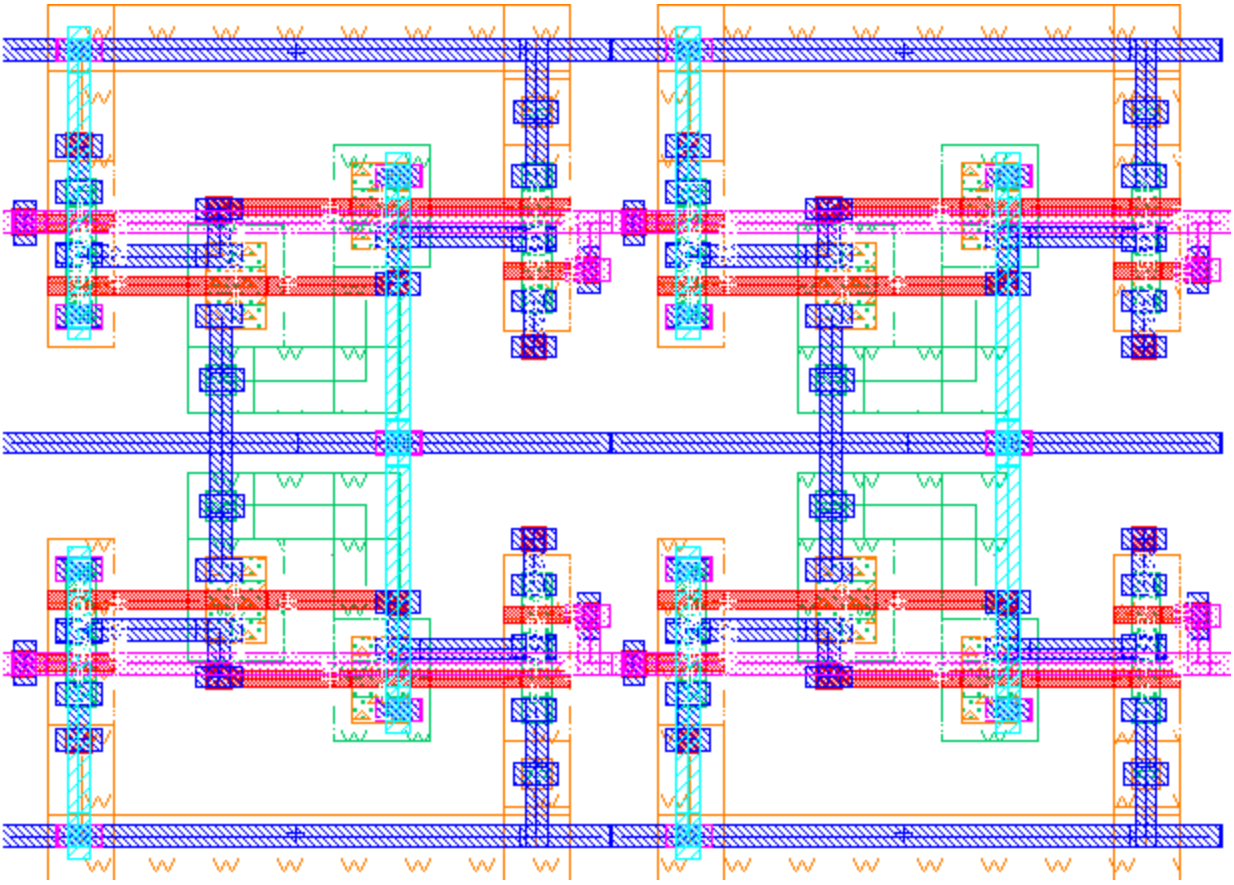

Figure 19: 2x2 SRAM Array

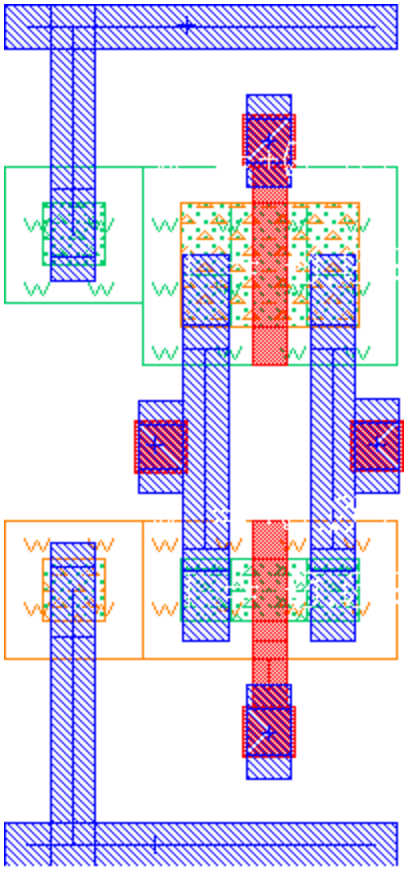

Figure 20: Layout of Transmission Gate

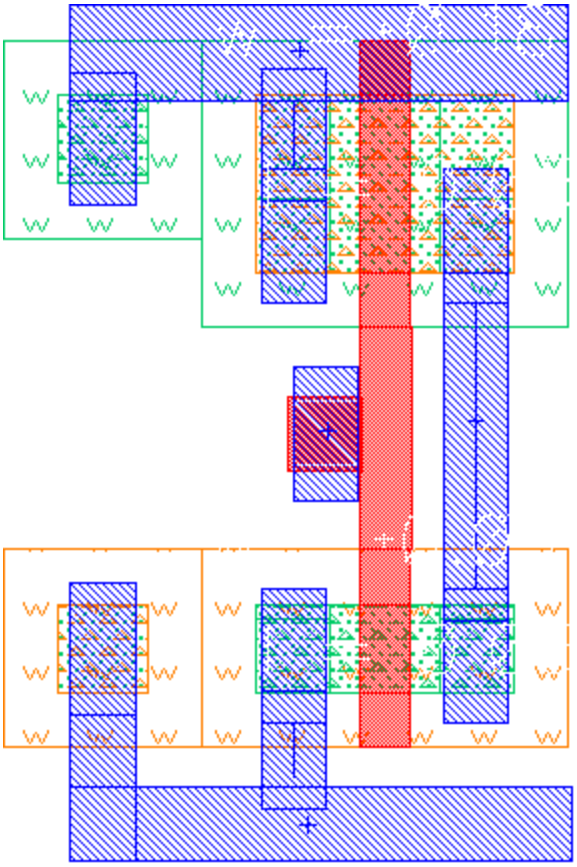

Figure 21: Layout of Inverter